AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) The semiconductor device according to claim [[1]] 8, wherein the first power supply line is linear and connects the first and third power supply terminals.

3. (Currently Amended) The semiconductor device according to claim [[1]] 8, wherein the second power supply line is linear and connects the second and fourth power supply terminals.

4. (Currently Amended) The semiconductor device according to claim [[1]] 8, wherein the second standard cell is arranged outside the ~~at least one function block~~ plurality of blocks.

5. (Currently Amended) The semiconductor device according to claim [[1]] 8, wherein the level converter cell is arranged in the ~~at least one function block~~ plurality of blocks.

6. (Currently Amended) The semiconductor device according to claim [[1]] 8, ~~further comprising~~ wherein the plurality of blocks is a plurality of function blocks, wherein the second standard cell is arranged between the plurality of function blocks.

7. (Currently Amended) The semiconductor device according to claim [[1]] 8, ~~further comprising~~ wherein the plurality of blocks is a plurality of function blocks, wherein the first standard cell and the level converter cell are arranged in each of the function blocks.

8. (Original) A semiconductor device comprising:

a plurality of blocks including a first block and a second block;

a plurality of first standard cells, wherein at least one of the first standard cells is arranged in the first block and at least one of the first standard cells is arranged in the second block, each of the first standard cells having a first power supply terminal;

a second standard cell arranged between the first and second blocks, wherein the second standard cell has a second power supply terminal misaligned with the first power supply terminal; and

at least one level converter cell aligned with the first and second standard cells and having a third power supply terminal aligned with the first power supply terminal and a fourth power supply terminal aligned with the second power supply terminal.

9. (Original) The semiconductor device according to claim 8, further comprising a third block arranged between the first and second blocks, wherein the second standard cell is arranged in the third block.

10. (Original) The semiconductor device according to claim 8, wherein the at least one level converter cell is arranged in at least one of the first and second blocks.

11. (Original) The semiconductor device according to claim 8, wherein the at least one level converter cell is arranged between the first and second blocks.

12. (Original) The semiconductor device according to claim 8, further comprising:

a first power supply line connected to the first power supply terminal of each of the first standard cells arranged in the first and second blocks; and

a second power supply line connected to the second power supply terminal of the second standard cell.

13. (Original) The semiconductor device according to claim 8, further comprising:

a first power supply line connected to the first power supply terminal of the first standard cell arranged in the first block;

a second power supply line connected to the first power supply terminal of the first standard cell arranged in the second block; and

a third power supply line connected to the second power supply terminal of the second standard cell.

14. (Original) The semiconductor device according to claim 8, further comprising a linear first power supply line connected to the first power supply terminal of at least one of the plurality of first standard cells and to the third power supply terminal of the at least one level converter cell.

15. (Original) The semiconductor device according to claim 8, further comprising a linear second power supply line connected to the second power supply terminal of the second standard cell and the fourth power supply terminal of the at least one level converter cell.

16. (Original) A designing apparatus for generating layout data of a semiconductor device, wherein the semiconductor device is provided with a plurality of blocks including a first block and a second block, a plurality of first standard cells arranged in the first and second blocks, a second standard cell arranged between the first and second blocks, and at least one level converter cell, the plurality of first standard cells, the second standard cell, and the level converter cell each having an end, a first region separated from the end by a predetermined first distance, and a second region separated from the end by a predetermined second distance, wherein each of the first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second power supply terminal formed in the second region, and the level converter cell has a third power supply terminal formed in the first region and a fourth power supply terminal formed in the second region, the designing apparatus comprising:

a processor, wherein the processor obtains netlist data of the semiconductor device, sets a power supply voltage of each of the blocks based on the netlist data, sets a voltage between the blocks based on the power supply voltage of each block, generates the level converter cell based on the voltage between the blocks, and arranges the level converter cell in one of locations in or between the blocks in accordance with the power supply voltage and the voltage between the blocks so as to align the level converter cell with the first and second standard cells.

17. (Original) The designing apparatus according to claim 16, wherein the processor arranges the level converter cell in a block having a power supply voltage that differs from the voltage between the blocks.

18. (Original) The designing apparatus according to claim 16, wherein the processor further aligns the first and second standard cells with the level converter cell.

19. (Original) A computer readable storage medium storing a program for generating layout data of a semiconductor device having a plurality of blocks with a computer, wherein the semiconductor device is provided with a plurality of blocks including a first block and a second block, a plurality of first standard cells arranged in the first and second blocks, a second standard cell arranged between the first and second blocks, and at least one level converter cell, the plurality of first standard cells, the second standard cell, and the level converter cell each having an end, a first region separated from the end by a predetermined first distance, and a second region

separated from the end by a predetermined second distance, wherein each of the first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second power supply terminal formed in the second region, and the at least one level converter cell has a third power supply terminal formed in the first region and a fourth power supply terminal formed in the second region, the program comprising the steps of:

obtaining netlist data of the semiconductor device with the semiconductor device;

setting a power supply voltage of each of the blocks based on the netlist data;

setting a voltage between the blocks based on the power supply voltage of each block;

generating the level converter cell based on the voltage between the blocks; and

arranging the level converter cell in one of locations in or between the blocks in accordance with the power supply voltage and the voltage between the blocks so as to align the level converter cell with the first and second standard cells.

20. (Original) A semiconductor device comprising:

a linear first power supply line for supplying a first power supply voltage;

a linear second power supply line extending parallel to the first power supply line for supplying a second power supply voltage that differs from the first power supply voltage;

a first block;

a second block;

a plurality of first standard cells arranged in each of the first and second blocks, wherein each of the plurality of first standard cells has a predetermined shape and includes an end and a first power supply terminal formed at a location separated from the end by a predetermined first distance, the first power supply terminal being connected to the first power supply line;

a second standard cell having substantially the same shape as the first standard cells and including an end and a second power supply terminal formed at a location separated from the end by a predetermined second distance that differs from the first distance, the second power supply terminal being connected to the second power supply line; and

a level converter cell aligned with the first and second standard cells, wherein the level converter cell has substantially the same shape as the first and second standard cells and includes an end, a third power supply terminal formed at a location separated from the end by the first distance and connected to the first power supply line, and a fourth power supply terminal formed at a location separated from the end by the second distance and connected to the second power supply line.